Advanced Topics on Design of Analog Integrated Circuits
(Graduate Intensive Course)

June 29th - July 14th, 2015
18-22 hours, Monday-Friday
Classroom F-101, ITESO campus

Instructor Information

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Jaime Ramírez-Angulo is currently Klipsch Distinguished Professor, Distinguished Award Professor, IEEE Fellow, and Director of the Mixed-Signal VLSI Lab at the Klipsch School of Electrical and Computer Engineering, New Mexico State University (Las Cruces, New Mexico), USA. He received a degree in Communications and Electronic Engineering (Professional degree), an M.S.E.E. from the National Polytechnic Institute in Mexico City and a Dr.-Ing degree from the University of Stuttgart, Germany, in 1975, 1977, and 1982 respectively. He was professor at the National Institute for Astrophysics Optics and Electronics (INAOE) and at Texas A&M University. His research is related to various aspects of design and test of analog and mixed-signal Very Large Scale Integrated Circuits. He has made numerous contributions to this field which have been reported in over five hundred publications in the most prestigious journals and conferences in analog circuit design. His papers have 4,300 citations. He has an H-index larger than 20 in ISI (Science Citation Index) and 30 in Google scholar. He has two high technology patents and has held numerous invited and keynote presentations. He has been a consultant to Texas Instruments, NASA-ACE, NASA-Ames, NASA Goddard and Oak Ridge National Laboratories. His research has been supported by National Science Foundation, Sandia National Labs, Los Alamos National Labs, Engineering Foundation, Texas Instruments and Agilent. He received the prestigious URC University Research Council for exceptional achievements in creative scholarly activities and the Westhafer award for Excellence in Research and Creativity in 2002. In 2002 he was named Paul W. Klipsch Distinguished Professor and was IEEE distinguished lecturer for the period 2003-2005. He was named Distinguished Award Professor in August 2012. Two of his papers were listed in 2005 among the 100 most downloaded papers of all IEEE societies. In May 2004 one of his students earned the award as most outstanding Ph.D. student and in 2006 and 2007 two of his students earned the award as most outstanding M.Sc. students at New Mexico State University. He was a Fulbright scholar for the period September 2009-May 2010 and was in the IEEE Circuits and Systems Fellow Selection Committee in 2009. In September 2014 he was awarded Level III (highest level) membership in the Mexican National System of Researchers (Sistema Nacional de Investigadores or SNI).

General Description

In this course we address the state of the art as well as advanced topics in the field of analog integrated circuit design. We also revisit fundamental theoretical concepts. The main topics covered in the course will be complemented through seven practical laboratories. A comprehensive final project consisting on the design of an analog integrated circuit with some advanced feature is required to pass this course; this is
done starting from design specifications and it requires the student to go over each step of the design cycle: initial device sizing, computer simulations, design optimization, layout of the integrated circuit, and circuit extraction. Cadence design suite and 180 nm CMOS technology will be intensively used in this course.

This graduate course grants 8 credits to students officially registered to an ITESO graduate program, and grants a diploma for external students.

**Prerequisites**

It is assumed the student is familiar with the basic functionality of Cadence Integrated Circuit Design Framework and with the basic building blocks of analog integrated circuits as well as with the design of one stage and two stage op-amps.

**Objectives**

By the end of the course the student will be able to:

A. Analyze the design procedure of single-ended and fully differential op-amps (ANALYSIS).
B. Design and simulate fully differential one-stage and two-stage op-amps (SYNTHESIS).
C. Identify floating gate and quasi floating gate techniques (COMPREHENSION).
D. Analyze class AB op-amps and super class AB op-amps (ANALYSIS).
E. Design a class AB op-amp based on the free class AB technique (SYNTHESIS).
F. Design rail to rail op-amps with constant transconductance (SYNTHESIS).
G. Apply gain boosting techniques to design an ultra-high gain op-amp (APPLICATION).
H. Apply techniques to improve CMRR for designing op-amps with enhanced CMRR (APPLICATION).
I. Design a linear operational transconductance amplifier (SYNTHESIS).
J. Identify the applications of offset compensation techniques and feedforward wideband amplifiers (COMPREHENSION).
K. Design of offset compensated op-amp (SYNTHESIS).
L. Identify analog multipliers and feedforward wideband amplifiers (COMPREHENSION).
M. Identify applications of analog blocks such as: buffers, flipped voltage followers super buffers (COMPREHENSION).
N. Identify applications of advanced design techniques such as: high performance current mirrors, current mode op-amps, current mode signal processing, low voltage techniques, winner-take-all and median circuits (ANALYSIS).
O. Identify the noise in op-amps and techniques to correct it (ANALYSIS).
P. Formulate and implement a project consisting on the design of an analog integrated circuit with some innovative feature (SYNTHESIS).
Q. Efficiently exploit commercially available CAD tools for integrated circuit modeling and design (APPLICATION).

General Contents

1) Review: Step by step design of single-ended and fully differential one stage and two stage op-amps
2) Floating gate and quasi floating gate techniques
3) Class AB op-amps and super class AB op-amps
4) Rail to rail op-amps
5) Gain boosting techniques: ultra-high gain op-amps
6) Techniques to improve CMRR
7) Linear transconductors
8) Offset compensation techniques
9) Feedforward wideband amplifiers
10) Analog multipliers
11) Buffers, flipped voltage followers super buffers
12) High performance current mirrors and current mode op-amps
13) Current mode signal processing
14) Low voltage techniques
15) Winner-take-all and median circuits
16) Noise in op-amps

Laboratories:

Lab 1: Design and simulation of fully differential one stage and two stage op-amps
Lab 2: Design of a class AB op-amp based on the free class AB technique
Lab 3: Design of a rail to rail op-amp with constant transconductance
Lab 4: Design of an ultra-high gain op-amp
Lab 5: Design of op-amps with enhanced CMRR
Lab 6: Design and simulation of linear operational transconductance amplifier
Lab 7: Design of offset compensated op-amp
Lab 8: Final project

Relationship between Contents and Objectives

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Course Skeleton

For the proposed course skeleton it is assumed: a group of 5 to 18 students; daily 4-hour class meetings during approximately 12 days; and simulation software available at ITESO (Cadence design suite).

*It is also expected that the student will be able to dedicate an average of 10 hours of work per day to this course, including attending classes (4 hours per class plus 6 hours of independent work). This graduate course grants 8 credits to ITESO graduate students and a diploma for external students.*

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Assessment

The overall grade in this course will be built from the following elements:

- Laboratories  60%
- Project        35%
- Participation  5%

Each student will realize a final project during the course. The topic chosen must be approved by the instructor. The final project report must be submitted following a template that will be indicated in the course. Depending on the selected topic and class size, the project can be realized individually or in teams of up to 2 students. Further instructions about the final project report and corresponding technical presentation will be delivered during the course.

Quality of students’ participation during the lectures will be graded. This participation will be evaluated based on student’s attitude and performance during class: punctuality, willingness to ask relevant questions, respect to others, attention during class, ability to answer questions, etc.

Teaching Methods

This course will use a variety of teaching methods including: lecturing, readings, computer simulations and labs, project report writing and self-conducted laboratory work.

Important information related to the course will be posted in the Moodle web site at the beginning of this
course. Open and frequent communication with the instructor is encouraged. Collaboration between the students is also encouraged.

The course will be conducted in Spanish, however, all of the written material for the course will be available in English.

Resources

Instructor’s web site

http://ece.nmsu.edu/faculty-staff/jairamir/

Reference books:


Introduction to CMOS op-amps Roubik Gregorian, Wiley Interscience, 1999, ISBN: 0-471-31778-0 (available as ebook at NMSU library)


Cadence IC design suite:

Cadence® Design Framework Integrator’s Toolkit
Virtuoso® Schematic Editor – XL,
Virtuoso® Analog Design Environment – XL,
Virtuoso® Analog Design Environment – GXL,
Spectre Extensive Partitioned Simulator,
Virtuoso® Multi-mode Simulation with Spectre XPS,
Virtuoso® Layout Suite – GXL,
Diva® Physical Verification (DRC, LVS, ERC) and Extractor Suite,

NOTA: En caso de alguna dificultad o confusión respecto de este programa de estudios (por estar en idioma inglés), favor de consultar directamente con el Dr. Esteban Martínez Guerrero (margres@iteso.mx).